

## 100mA Charge Pump Voltage Converter with Shutdown

### Features:

- Optional High-Frequency Operation Allows Use of Small Capacitors
- Low Operating Current (FC = GND):
  - 50  $\mu$ A
- High Output Current (100 mA)
- Converts a 2.4V to 5.5V Input Voltage to a Corresponding Negative Output Voltage (Inverter mode)
- Uses Only 2 Capacitors; No Inductors Required
- Selectable Oscillator Frequency:
  - 10 kHz to 200 kHz
- Power-Saving Shutdown Input
- Available in 8-Pin MSOP, 8-Pin PDIP and 8-Pin Small Outline (SOIC) Packages

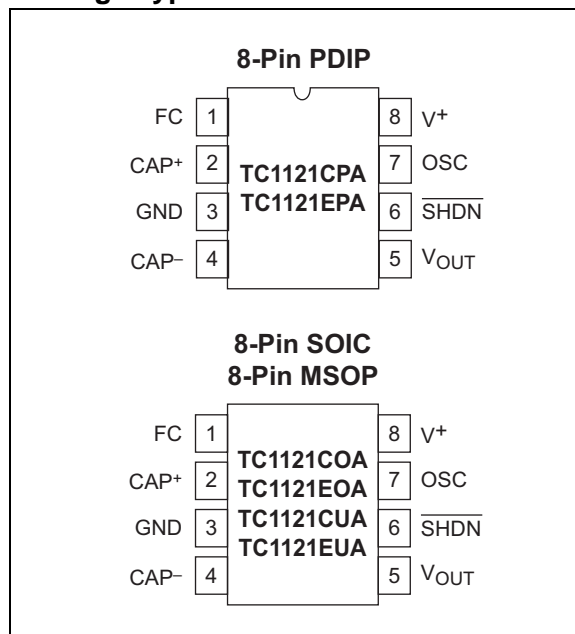
### Applications:

- Laptop Computers
- Medical Instruments
- Disk Drives
- $\mu$ P-Based Controllers
- Process Instrumentation

### Device Selection Table

Part Number	Package	Operating Temp. Range
TC1121COA	8-Pin SOIC	0°C to +70°C
TC1121CPA	8-Pin PDIP	0°C to +70°C
TC1121CUA	8-Pin MSOP	0°C to +70°C
TC1121EOA	8-Pin SOIC	-40°C to +85°C
TC1121EPA	8-Pin PDIP	-40°C to +85°C
TC1121EUA	8-Pin MSOP	-40°C to +85°C

### Package Type



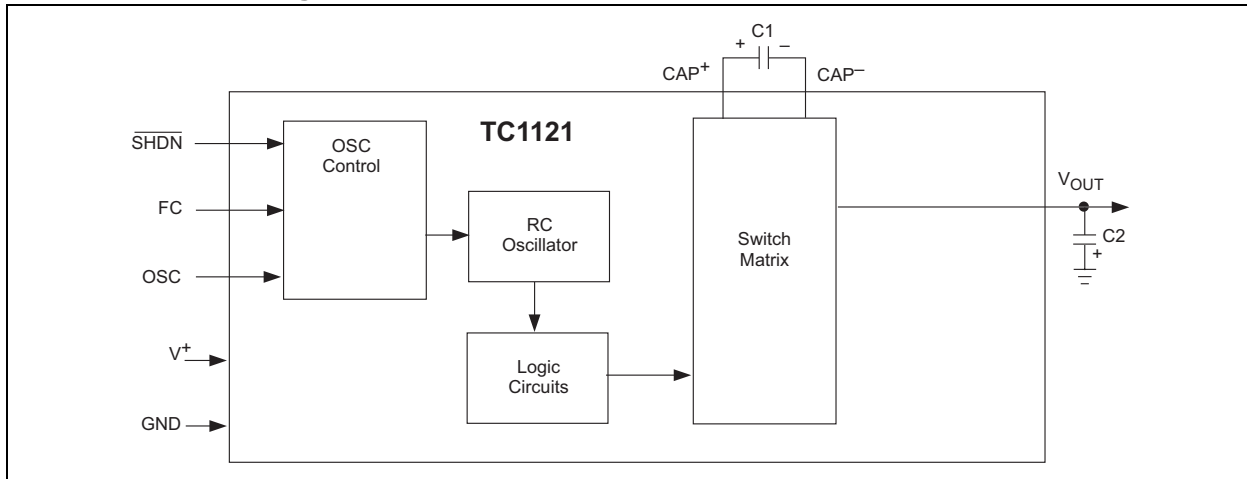
### General Description:

The TC1121 is a charge pump converter with 100 mA output current capability. It converts a 2.4V to 5.5V input to a corresponding negative output voltage. As with all charge pump converters, the TC1121 uses no inductors saving cost, size and EMI.

An on-board oscillator operates at a typical frequency of 10 kHz (at V<sup>+</sup> = 5V) when the frequency control input (FC) is connected to ground. The oscillator frequency increases to 200 kHz when FC is connected to V<sup>+</sup>, allowing the use of smaller capacitors. Operation at sub-10 kHz frequencies results in lower quiescent N<sub>S</sub>current and is accomplished with the addition of an external capacitor from OSC (pin 7) to ground. The TC1121 also can be driven from an external clock N<sub>S</sub>connected OSC. Typical supply current at 10 kHz is 50  $\mu$ A, and falls to less than 1  $\mu$ A when the shutdown input is brought low, whether the internal or an external clock is used. The TC1121 is available in 8-pin SOIC, MSOP and PDIP packages.

# TC1121

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings\*

Supply Voltage ( $V_{DD}$ )	6V
OSC, FC, SHDN Input Voltage	-0.3V to ( $V^+ + 0.3V$ )
Output Short Circuit Duration	10 Sec.
Package Power Dissipation ( $T_A \leq 70^\circ\text{C}$ )	
8-Pin PDIP	730 mW
8-Pin SOIC	470 mW
8-Pin MSOP	333 mW
Operating Temperature Range	
C Suffix	0°C to +70°C
E Suffix	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### TC1121 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ (C suffix), $-40^\circ\text{C}$ to $+85^\circ\text{C}$ (E suffix), $V^+ = 5V \pm 10\%$ $C_{OSC} = \text{Open}$ , $C1, C2 = 10 \mu\text{F}$ , $\text{FC} = V^+$ , $\text{SHDN} = V_{IH}$ , typical values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.						
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$I_{DD}$	Active Supply Current	—	50 0.6	100 1	$\mu\text{A}$ mA	$R_L = \text{Open}$ , $\text{FC} = \text{Open}$ or $\text{GND}$ $R_L = \text{Open}$ , $\text{FC} = V^+$
$I_{SHUTDOWN}$	Shutdown Supply Current	—	0.2	1.0	$\mu\text{A}$	$\text{SHDN} = 0V$
$V^+$	Supply Voltage	2.4	—	5.5	V	
$V_{IH}$	SHDN Input Logic High	$V_{DD} \times 0.8$	—	—	V	
$V_{IL}$	SHDN Input Logic Low	—	—	0.4	V	
$I_{IN}$	Input Leakage Current	-1 -4	—	1 4	$\mu\text{A}$	SHDN, OSC FC pin
$R_{OUT}$	Output Source Resistance	—	12	20	$\Omega$	$I_{OUT} = 60 \text{ mA}$
$I_{OUT}$	Output Current	60	100			$V_{OUT} = \text{more negative than } -3.75V$
$F_{OSC}$	Oscillator Frequency	5 100	10 200	— —	kHz	Pin 7 Open, Pin 1 Open or $\text{GND}$ $\text{SHDN} = V_{IH}$ , Pin 1 = $V^+$
$P_{EFF}$	Power Efficiency	— 93 94 —	— 97 97 92	— — —	%	$\text{FC} = \text{GND}$ for all $R_L = 2k$ between $V^+$ and $V_{OUT}$ $R_L = 1k\Omega$ between $V_{OUT}$ and $\text{GND}$ $I_L = 60 \text{ mA}$ to $\text{GND}$
$V_{EFF}$	Voltage Conversion Efficiency	99	99.9	—	%	$R_L = \text{Open}$

**Note 1:** Connecting any input terminal to voltages greater than  $V^+$  or less than  $\text{GND}$  may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC1121.

# TC1121

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## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

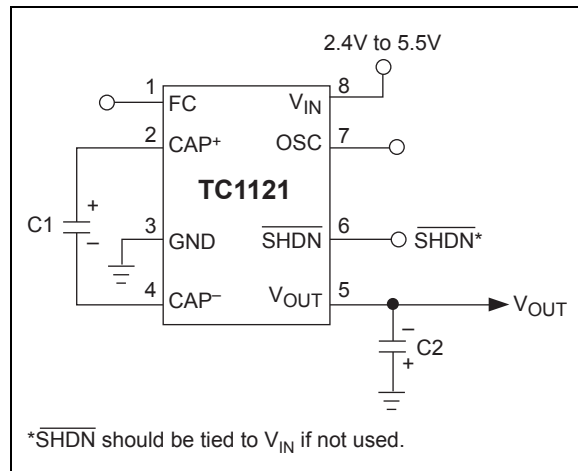
**TABLE 2-1: PIN FUNCTION TABLE**

Pin No. (8-Pin MSOP, PDIP, SOIC)	Symbol	Description
1	FC	Frequency control for internal oscillator, FC = open, $F_{OSC} = 10 \text{ kHz typ}$ ; FC = $V^+$ , $F_{OSC} = 200 \text{ kHz typ}$ ; FC has no effect when OSC pin is driven externally.
2	CAP <sup>+</sup>	Charge-pump capacitor, positive terminal.
3	GND	Power-supply ground input.
4	CAP <sup>-</sup>	Charge-pump capacitor, negative terminal.
5	OUT	Output, negative voltage.
6	$\overline{\text{SHDN}}$	Shutdown.
7	OSC	Oscillator control input. An external capacitor can be added to slow the oscillator. Take care to minimize stray capacitance. An external oscillator also may be connected to overdrive OSC.
8	$V^+$	Power-supply positive voltage input.

## 3.0 APPLICATIONS

### 3.1 Negative Voltage Converter

The TC1121 is typically used as a charge-pump voltage inverter. C1 and C2 are the only two external capacitors used in the operating circuit (Figure 3-1).



**FIGURE 3-1:** Charge Pump Inverter

The TC1121 is not sensitive to load current changes, although its output is not actively regulated. A typical output source resistance of 11.8Ω means that an input of +5V results in -5V output voltage under light load, and only decreases to -3.8V typ with a 100 mA load.

The supplied output current is from capacitor C2 during one-half the charge-pump cycle. This results in a peak-to-peak ripple of:

$$V_{\text{RIPPLE}} = I_{\text{OUT}}/2(f_{\text{PUMP}}) (C2) + I_{\text{OUT}} (ESR_{C2})$$

Where  $f_{\text{PUMP}}$  is 5 kHz (one half the nominal 10 kHz oscillator frequency), and  $C2 = 150 \mu\text{F}$  with an ESR of 0.2Ω, ripple is about 90 mV with a 100 mA load current. If C2 is raised to 390 μF, the ripple drops to 45 mV.

### 3.2 Changing Oscillator Frequency

The TC1121's clock frequency is controlled by four modes:

**TABLE 3-1: OSCILLATOR FREQUENCY MODES**

FC	OSC	Oscillator Frequency
Open	Open	10 kHz
FC = V <sup>+</sup>	Open	200 kHz
Open or FC = V <sup>+</sup>	External Capacitor	See Typical Operating Characteristics
Open	External Clock	External Clock Frequency

The oscillator runs at 10 kHz (typical) when FC and OSC are not connected. The oscillator frequency is lowered by connecting a capacitor between OSC and GND, but FC can still multiply the frequency by 20 times in this mode.

An external clock source that swings within 100 mV of V<sup>+</sup> and GND may overdrive OSC in the Inverter mode. OSC can be driven by any CMOS logic output. When OSC is overdriven, FC has no effect.

Note that the frequency of the signal appearing at CAP<sup>+</sup> and CAP<sup>-</sup> is half that of the oscillator. In addition, by lowering the oscillator frequency, the effective output resistance of the charge-pump increases. To compensate for this, the value of the charge-pump capacitors may be increased.

Because the 5 kHz output ripple frequency may be low enough to interfere with other circuitry, the oscillator frequency can be increased with the use of the FC pin or an external oscillator. The output ripple frequency is half the selected oscillator frequency. Although the TC1121's quiescent current will increase if the clock frequency is increased, it allows smaller capacitance values to be used for C1 and C2.

### 3.3 Capacitor Selection

In addition to load current, the following factors affect the TC1121 output voltage drop from its ideal value 1) output resistance, 2) pump (C1) and reservoir (C2) capacitor ESRs and 3) C1 and C2 capacitance.

The voltage drop is the load current times the output resistance. The loss in C2 is the load current times C2's ESR; C1's loss is larger because it handles currents greater than the load current during charge-pump operation. Therefore, the voltage drop due to C1 is about four times C1's ESR multiplied by the load current, and a low (or high) ESR capacitor has a greater impact on performance for C1 than for C2.

In general, as the TC1121's pump frequency increases, capacitance values needed to maintain comparable ripple and output resistance diminish proportionately.

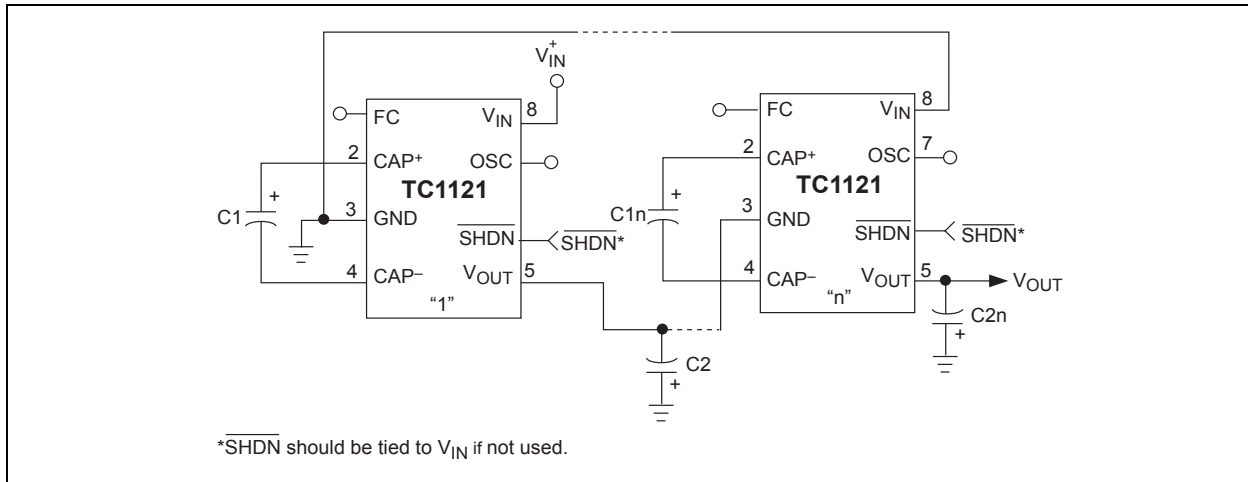
# TC1121

## 3.4 Cascading Devices

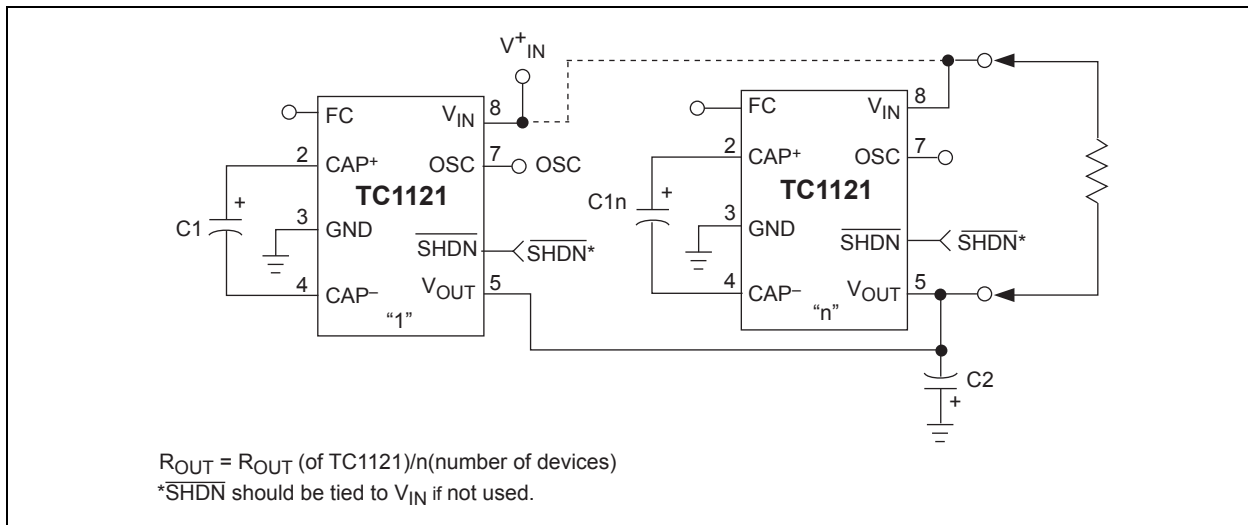
To produce greater negative magnitudes of the initial supply voltage, the TC1121 may be cascaded (see Figure 3-2). Resulting output resistance is approximately equal to the sum of individual TC1121  $R_{OUT}$  values. The output voltage (where  $n$  is an integer representing the number of devices cascaded) is defined by  $V_{OUT} = -n (V_{IN})$ .

## 3.5 Paralleling Devices

To reduce output resistance, multiple TC1121s may be paralleled (see Figure 3-3). Each device needs a pump capacitor  $C1$ , but the reservoir capacitor  $C2$  serves all devices. The value of  $C2$  should be increased by a factor of  $n$  (the number of devices).



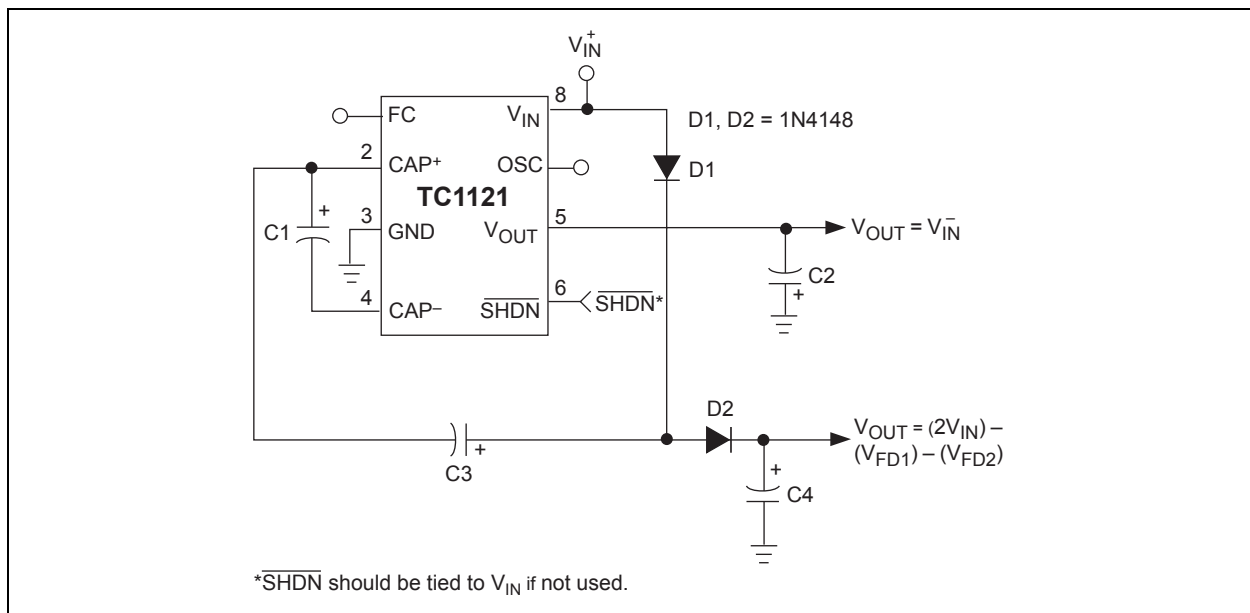
**FIGURE 3-2:** Cascading TC1121s to Increase Output Voltage



**FIGURE 3-3:** Paralleling TC1121s to Reduce Output Resistance

## 3.6 Combined Positive Supply Multiplication and Negative Voltage Conversion

Figure 3-4 shows this dual function circuit, in which capacitors C1 and C2 perform pump and reservoir functions to generate negative voltage. Capacitors C3 and C4 are the respective capacitors for multiplied positive voltage. This particular configuration leads to higher source impedances of the generated supplies due to the finite impedance of the common charge-pump driver.



**FIGURE 3-4:** Combined Positive Multiplier and Negative Converter

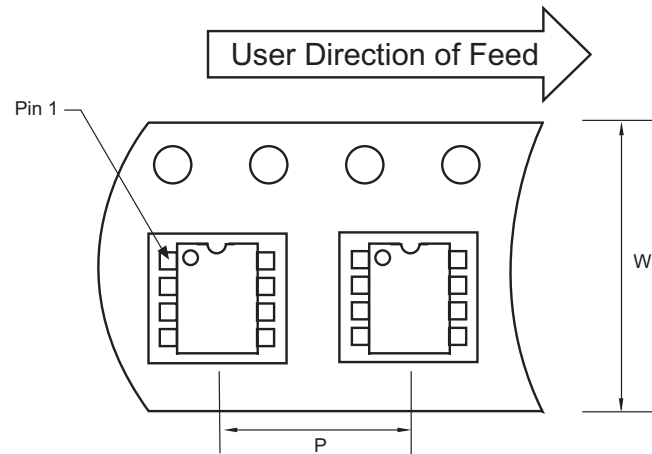
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

Package marking data not available at this time.

### 4.2 Taping Form

#### Component Taping Orientation for 8-Pin MSOP Devices

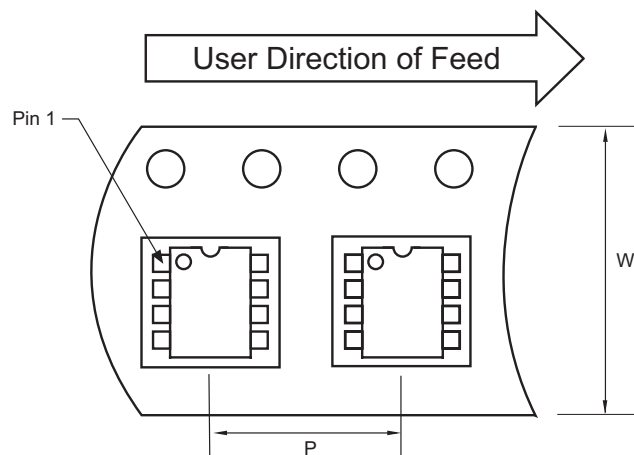


Standard Reel Component Orientation  
for 713 Suffix Device

#### Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

#### Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation  
for 713 Suffix Device

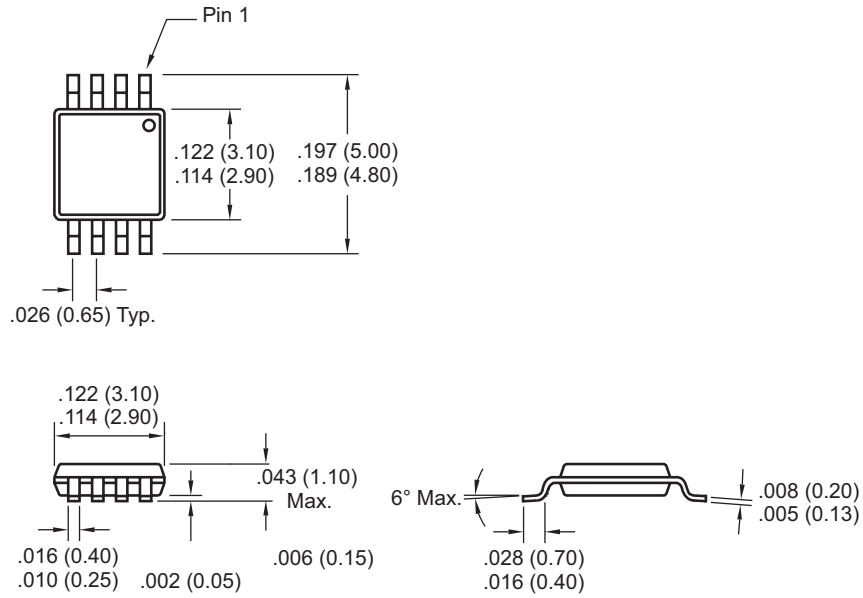
#### Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in



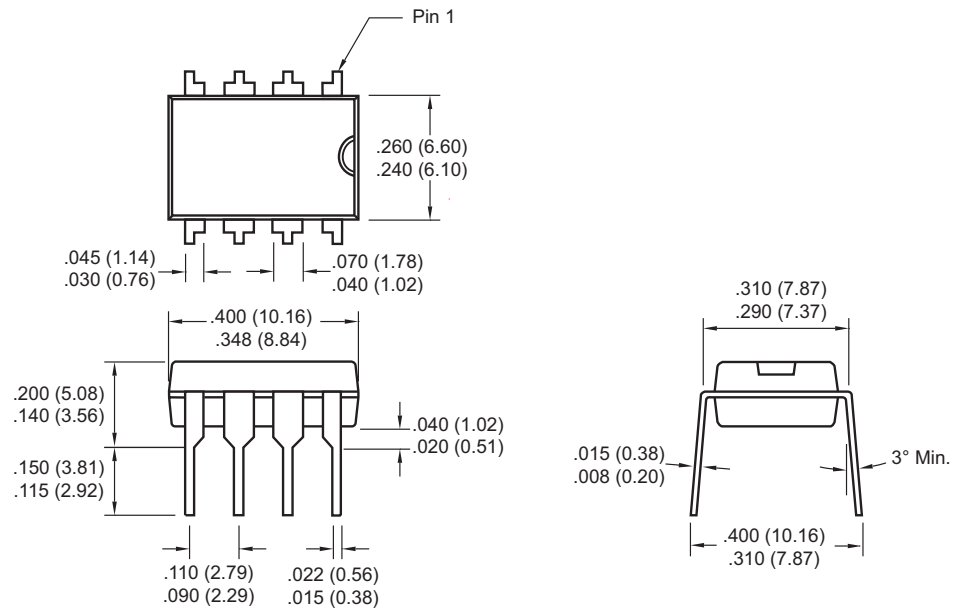
## 4.3 Package Dimensions

### 8-Pin MSOP



Dimensions: inches (mm)

### 8-Pin Plastic DIP

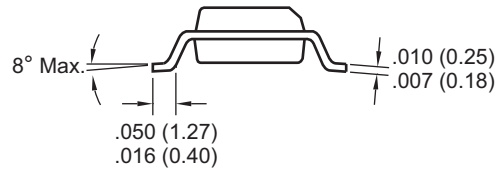
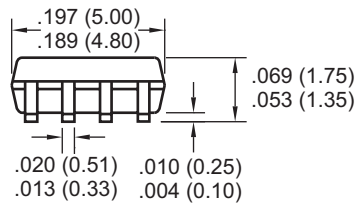
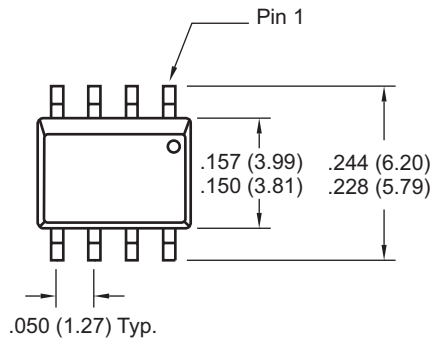


Dimensions: inches (mm)

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## Package Dimensions (Continued)

### 8-Pin SOIC



Dimensions: inches (mm)

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